**Project 9811-5: Progress Report, 1999 - 2001**

# Hierarchical Design and Analysis of Timed Systems

Wang Yi
Dept. of Computer Systems
Uppsala University

## 1 Comparision between Project Plan and Results

This project was started in January, 1999 with one Ph.D. student (Alexandre David 80%). The main scientific contributions of the project so far are:

- **3 papers accepted for publication** in international conference and workshops and **2 technical reports** and
- **3 prototype implemenations**:
- a prototype in Java to translate UML hierarchical models to UPPAAL models and
- a prototype in Java of a user interface UL for hierarchical modells,
- a prototype in C, CVODE and Java of a real time animator for dynamical systems.

The project is to develop techniques and languages for hierarchical modelling and analysis. In particular, we planned to develop a modelling Language and user interface for UPPAAL for handling hierarchical models, that is not supported by the current implementation of UPPAAL. We have been following the orginal plan. A prototype language (named UL) for hierarchical modelling has been designed and implimented in Java.

## 2 A list of Publications

- Formal Verification of UML Statecharts with Real-time Extensions, David Alexandre, Möller M. Oliver, and Wang Yi, IT report, Department of Information Technology, 2001.
- From Hierarichcal Timed Automata to UPPAAL, David Alexandre and Möller M. Oliver, BRICS report RS-01-11, Department of Computer Science, Åhus University, Denmark, 2001.
- A Real Time Animator for Hybrid Systems. Tobias Amnell, Alexandre David, and Wang Yi. To appear in the proceedings of 6th ACM SIGPLAN LCTES'2000.

- Modelling and Analysis of a Field Bus Protocol. Alexandre David and Wang Yi. In the proceedings of the 12th Euromicro Conference On ReaL-Time Systems, Stockholm, Sweden June 19th-21th , 2000.

- Hierarchical Timed Automata. Alexandre David and Wang Yi. Tech Report, Department of IT, Uppsala University, March, 2000. Presented at the international workshop on Specification, Implementation and Verification of Object-Oriented Embedded Systems, Cannes, France, June 2000.

## 3 Research Directions

A real-time system often contain a number of processes constituting a network. Many of the existing verification tools e.g. Kronos, HyTech and UPPAAL are designed to model the processes as a flat network and search through all the possible combinations of local states of the processes. This restricts the applicability of these tools to real-world systems that often contain hundreds or thousands of processes. It is in practice impossible for them to deal with such huge networks of processes due to the state-space explosion problem. A crucial observation is that the processes may be in many cases partitioned into classes. Processes in each of the classes may be analyzed separately from the other classes. The procedure may be continued within each class. This is the so-called hierarchical analysis. Unfortunately, there is few automatic verification tool supporting this type of analysis. We mention a few examples. SMV models a system e.g. a hardware circuit as a huge binary decision diagram with no structural information at all. The validation tool SDT for SDL only supports two-level hierarchy; but SDT is basically a simulation tool. Similarly STATEMATE based on state-charts supports hierarchical modelling and simulation to some extent; but no model-checker is available, in particular, for checking real-time properties.

The first step of the project was planned to develop a modelling language to model and simulate hierarchical structures. A prototype (named UL++) is currently available. We plan to finalize the implementation of UL in Java and integrate it with the UPPAAL tool. Hopefully, in the short future, it will replace the current UPPAAL description language and user interface. We should point out that the UL project is naturally related to the existing code-generation project supported by ARTES as both address language design issues and more importantly the code-generation project is to generate runnable codes from design specifications written in UL. The future plan with the UL–project is to develop verification techniques that utilize the hierarchical information in order to guide the state–space exploration algorithm that the UPPAAL engine is based on and to introduce abstraction in the UPPAAL simulator and diagnostic trace–generator.

## 4 Industrial Collaboration

We have been collaborating with ABB Automation Products to study a field bus protocol. Our goal is to study the hierarchical structure of the protocol to guide the design of UL. In 1999 and 2000, there have been regular visits between ABB Automation Products (Ulf Hammar) and members (Alexandre David and Wang Yi) of this project. We cite the statement by our industrial collaborator: *the techniques and methods provided by Uppsala University are very promising, 2000 May, Ulf Hammar, ABB Automation Products.*