Project 9811-5: **Application for Prolongation for 2001-2003**

# Hierarchical Design and Analysis of Timed Systems

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## 1 Summary

This document is an application for prolongation for Hierarchical Design and Analysis of Timed Systems for Prolongation for 2001-2003. The goal of the project is to further develop the UPPAAL tool to a *coherent tool environment* for the development of embedded real-time systems, which supports each step of the system development process, from *specification, design, simulation, verification, runnable code generation, to test generation.*

## 2 Research Topics

Currently, the tool UPPAAL provides no support for modelling hierarchical structures, not to mention hierarchical analysis. The user can describe only a network of automata in the very flat form, which restricts the size of problems that UPPAAL can deal with. In the past two years we have successfully carried out a case-study with ABB Industrial Products to model and verify a bus protocol (AF 100) developed by ABB Industrial Systems AB, which is a commercial product. It is our experience with model-checkers like UPPAAL that a large part of the total time in most of the case studies is spent on constructing the system model, i.e., modeling. This has lead to a strong demand for a modelling language as well as a graphical user interface, with features supporting abstractions, such as hierarchical descriptions of models. There have been several modelling languages e.g. State-Chart for Statemate, developed particularly for modelling and simulation. However, rather little work has been done on static analysis for such languages to provide static information, e.g. types, hierarchical structures etc to guide verification.

We plan to develop an object–oriented modelling language as well as a graphical user interface for the tool UPPAAL. It supports two types of hierarchical structures:

Process hierarchy may be created within the network structure, i.e. the so-called classes of processes. The model-checker may utilize the class information to perform state-space searching locally within each class (hierarchy) until a synchronization point with another class is found. This may avoid the arbitrary global interleaving of the local transitions within the class. Some preliminary results on timed systems along this line have been reported in a paper presented at CONCUR98 ( available).

State hierarchy may be created within the process structure. A state of a particular process may consist of a number of other states that constitute another process with entry and exit states. The interesting information for a model-checker based on reachability analysis is the reachable entry and exit states. Such local processes (named super states in UL++) may be analyzed locally in a pre-processor to provide the information on entry and exit states

to the model-checker. Results along this line have been presented in a paper presented at RTSS'97 ( available). However the RTSS-paper only deals with a simple case i.e. each static loop as a super-state.

We should mention that this project is naturally related to the existing *code-generation* project supported by ASTEC as both address language design issues and more importantly the code-generation project is to generate runnable codes from design specifications.

The future plan is to develop verification techniques that utilize the hierarchical information in order to guide the state–space exploration algorithm that the UPPAAL engine is based on and to introduce *abstraction* in the UPPAAL simulator and diagnostic trace–generator.

# 3 Work Plan

### Planned Lic and Ph.D Defenses

1. Licentiate Defense is planned in September, 2001. A draft version of the thesis is available and enclosed in the progress report.

2. Ph.D defense is planned in the spring of 2003.

### Complementary Activities

There have been several related activities in Uppsala within the following projects:

1. The UPPAAL Model Checker (i.e. the UPPAAL project) (supported by VINNOVA)

2. The EC project WOODDES (supported by European Commission)

### Work Plan and Budget

We apply for continued funding for Alexandre David (Ph.D. student) for the next two years: 2001-2003 (the Budget should be calculated according to the ARTES standard)

### Industrial Cooperation

The success of the UPPAAL project have generated a number of industrial interests. However, we will conduct the project mainly in collaboration with ABB Industrial Products AB (Ulf Hammar, Tel: 021 34 3059.