

ARTES Project Proposal

Hardware/Software Codesign of Real-Time Systems

Zebo Peng and Anders Törne
Center for Embedded Systems Engineering (CESE)
Dept. of Computer and Information Science
Linköping University

Summary

This proposal describes a joint project of the Center for Embedded Systems Engineering (CESE) at Linköping University and Saab Dynamics AB. This project deals with system-level design methods and tools for mixed hardware/software systems, with special emphasis on real-time issues. The project is part of CESE's research in the area of engineering techniques for time and safety critical embedded systems.

We would like to apply for ARTES funding to support one Ph.D. student for a period of two + two years to develop hardware/software codesign techniques for real-time applications. In particular the student will concentrate on the development of methods and tools for the architecture selection problem. This entails formulating a hardware/software architecture model, developing a mapping strategy to map a real-time system specification into such an architecture, and designing methods and tools for the analysis of a given design based on the given architecture. The student will also study the problem of how to use the analysis results to guide the modification of the given architecture in such a way that the final architecture corresponds to the optimal design of the system specification. The final objective of the project is to develop techniques and tools to allow the designers to quickly explore the different design alternatives and find a cost-effective solution of mixed hardware/software implementations of a given real-time system.

The research work will be done in close cooperation with the industry and will use examples from the industrial partners to demonstrate the advantages of our developed methods. Officially, this project is defined as a joint project of CESE and Saab Dynamics AB, which are both ARTES nodes. Additionally, Saab AB and Volvo Technological Development will also be involved in part of the project.

1. Introduction and Problem Statement

Embedded systems make use of both off-the-shelf microprocessors and ASICs to implement specialized functions [Cam96]. They have a very wide range of applications, including process control and computer-integrated manufacturing systems, transportation systems (automotive control, train control, ship control, and traffic control), avionics systems, missile control systems, telephone and communications systems, medical instruments, and different microcomputer-controlled domestic appliances. Such systems consist, by their nature, of both software and hardware components [Wol94].

The development of such systems requires special design techniques to integrate electrical engineering, computer engineering, and software engineering. Integration is essential for the optimization and management of the complexity of embedded systems, the manifold interactions between the subsystems and evolutionary maintenance of reliable systems with adequate cost and performance. The creation of the Center for Embedded Systems Engineering (CESE) recently at Linköping University is an effort to combine research strengths in several disciplinary areas to deal with the heterogeneous nature of embedded systems engineering. CESE consists currently of two research laboratories: ESLAB (Embedded Systems Laboratory) and RTSLAB (Real-Time Systems Laboratory) and its main mission is to develop engineering techniques for time and safety critical embedded systems. CESE is running several research projects in this area, which are sponsored by NUTEK and the Swedish industry.

The aim of the joint project described in this proposal is to develop hardware/software codesign techniques for real-time applications. This is related to the common characteristics of embedded systems, namely that they must behave correctly both in terms of function and timing. In order to guarantee that both the function and timing of an embedded system is correct, extensive validation and verification is needed throughout the whole design and development process. Currently, much of this is done using traditional software testing and hardware simulation methods, but these are known to be both inefficient and error prone [Cam96]. Further, these methods can only be efficiently used in the later stages of the design process when the detailed design has mostly been done. This results in a situation that the early design decisions, such as architecture selection, hardware/software partitioning, scheduling, etc., which have high impact on the timing characteristics and cost of the final implementation, are made based on inadequate analysis of the designed system. Therefore, many problems are created early and discovered late when traditional methods are used. And it becomes very difficult to predict the time and cost of development, since the discovery of a problem in the testing and simulation phase can lead to major revisions of earlier stages in the design.

This project is intended to remedy the problems described above by developing a systematic design method for real-time systems consisting of both hardware and software components. Our main emphasis will be on architecture selection and tools to support design space exploration in the early design phases.

2. Objectives and Research Issues

Our ultimate objective is to develop a real-time system design environment which consists of a set of integrated design methods and tools to allow designers to quickly explore the design space and to produce optimized implementations. Such a design environment is illustrated in Figure 1 and originally proposed in [Axe97b]. The basic idea is to allow designers to start the design process with a system specification which does not prescribe the implementation details, such as what to be implemented in hardware and what to be implemented in software. The system specification will then be mapped into a hardware/software architecture model to allow efficient analysis of design parameters. The analysis results will be used to guide the selection or improvement of the implementation architecture, partitioning and scheduling.

The main features of the proposed design environment are as follows.

- It will deal with earlier design phases, and increase the predictability of both the design process and the operation of embedded real-time systems.
- It will provide a framework to allow the designers to find more cost effective and reliable implementations.
- It will provide tools to support the designers and shorten the time to market.

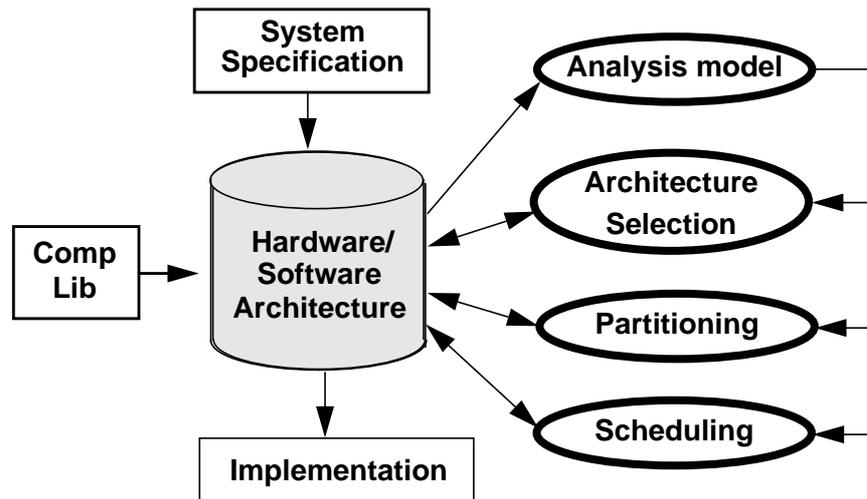


Figure 1. The proposed design environment.

The basic idea of the design environment discussed here and some theoretical results have been already developed and documented in Jakob Axelsson's Ph.D. thesis [Axe97b]. However, there are several research issues which remain to be solved and will be the main focus of the proposed project:

Specification techniques

We need to develop or select a specification formalism to support high-level and uniform specification of functionality and real-time requirements. The specification formalism should allow the analysis of a specification on a wide range of architecture models.

Heterogeneous architecture model

An essential component of the design environment is an architecture model to precisely capture the basic design structures developed typically at the early stages of the design process. Such a model should support the specification of the number and type of micro-processor, the ASICs and their features, memory, FPGAs, dedicated controllers, buses and the interconnect structure as well as the basic architecture for the ASICs. Different architecture models can be developed to fit into different application areas. For example, a distributed architecture model can be useful for some type of embedded systems while a centralized architecture can be more useful for the others.

One focus of our research will be on architecture models which are based on distributed network. Such architectures are widely used in automotive control and avionics systems as well as process control environments in the industry. And research in the co-design area, including [Axe97b], has neglected the issues related to distributed network. It is therefore very important to develop architecture models to support the analysis and design of real-time systems based on distributed networks. We will work closely with the industrial partners to develop such architecture models based on real-life industrial designs.

Analysis procedures

To be able to automate certain design activities, e.g. architecture selection and partitioning, it is essential to have good analysis procedures which can be used to predict the results of different alternative design decisions. Since the behavioral description of a real-time application normally contains several parallel tasks, the analysis must take into account the scheduling of tasks, i.e. how they share the hardware resources over time. Therefore, considerable effort has been put into developing flexible scheduling models for heterogeneous architectures, and a schedulability measurement which indicates how well a proposed design will meet its real-time constraints has been developed in [Axe95] [Axe97a]. The evaluation of the schedulability measurement requires that certain characteristics of a design, e.g. hardware area and execution time of different parts, can be estimated, and for this we need to develop analysis techniques and tools that can be applied to a wide range of architectures, including architectures which are based on distributed networks.

Synthesis

Once an analysis technique has been established, which can give indications about the quality of a proposed implementation, we can use this to automatically synthesize a good design. At Linköping University, we have developed several synthesis algorithms for the hardware/software partitioning problem [Axe96] [Axe97c] [Ele96] [Ele97]. In [Axe96], for example, a branch-and-bound algorithm which assigns tasks to processors and ASICs in the hardware architecture is described. In the proposed project, we can extend the existing tools of ours with further synthesis capabilities, especially for architecture synthesis, where different architectures are automatically generated from a set of hardware and software components.

Design re-use

Another important issue of the proposed research is to support incremental design and re-use of existing sub-systems. This means that we must have an efficient way of capturing existing sub-systems in the architecture model and develop techniques to perform incremental analysis of a design without having to start from scratch. Design re-use is an important issue for industrial application, since most of the designs in the industry are based on existing systems.

3. Expected Long-Term Results

The expected results of our research in the long run are:

- A formal notation for heterogeneous architecture, which can be executed or simulated.
- A technique to analyze execution time and implementation cost of a real-time system specification on different architectures, with emphasis on architectures based on distributed networks.
- A method to use the analysis results to support trade-offs between different architecture alternatives, e.g., software v. ASICs, different processors, and centralized v. distributed interconnect structure.
- A technique to support optimal architecture selection by formulating it as an optimization problem. Development of some heuristics to solve the combinatorial optimization problem.

The final result will be a coherent methodology for hardware/software co-design for embedded real-time applications and prototype support tools, which will be demonstrated with industrial examples.

4. Project Plan for the First Two Years

The main research of the project will be carried out by a Ph.D. student who is a member of CESE, with active involvement of Saab Dynamics which participates in the formulation of the problems, selection of industrial examples to be used as test cases, and evaluation of the results. The student is planned to spend 3 months in Saab Dynamics in a mobility program to get a better understanding of the problems in the industrial environment.

The main tasks to be executed in the first two years (Jan 1998 to Dec. 1999) are:

- Select a system specification language suitable for embedded real-time applications. This task will be carried out in connection to our research activity in System Specification which is currently sponsored by SSF.
- Develop a modeling technique for heterogeneous architecture, focusing on issues related to distributed networks. This will be the main research topic for the first year.
- Select and implement a partitioning algorithm for task allocation. This will be done based on some of our earlier research results and in connection to the COCODES project at ESLAB on hardware/software codesign which is sponsored by NUTEK's Embedded Systems program.
- Develop a technique for the analysis of execution time of tasks on different architectures.
- Develop rules to use the analysis result to manually modify the architecture.

The relation between the different activities of the first two years can be visualized in Figure 2. After the first two years, the results will be documented in the student's Lic. thesis. During the additional two years, the student will develop mainly a technique to automate the architecture modifications and synthesis pro-

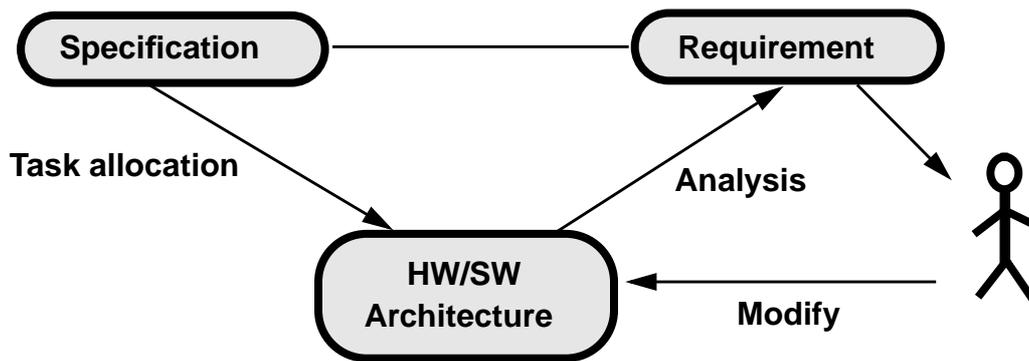


Figure 2. The main tasks of the first two years.

cedure, replacing the person illustrated in Figure 2.

5. Preliminary Budget

The preliminary yearly budget is calculated as follows:

Ph.D. Student, 80%	300.000 SEK
Supervisors (Peng, Törne), 10%	70.000 SEK
Computer and equipment	50.000 SEK
Travel	30.000 SEK
Administration and office	50.000 SEK
 Total budget per year:	 500.000 SEK

The project will last for 2 + 2 years.

6. CESE and Research Cooperation

This project is part of an effort to develop engineering techniques for time and safety critical embedded systems at CESE. CESE consists currently of ESLAB and RTSLAB at the Department of Computer and Information Science (IDA) which has extensive experience of research on real-time systems, formal methods and hardware/software codesign. One of the aims of the center is to make this competence available to the industry, and to develop it in directions which are of strategic importance. In particular, ESLAB's main research focuses on the development of design and test methodologies and tools for embedded systems, especially those which consist of tightly coupled hardware and software subsystems. RTSLAB, on the other hand, has a broad competence in the design of embedded software systems. ESLAB is also involved in ECSEL at Linköping University which is sponsored by SSF.

Both ESLAB and RTSLAB have involved and are participating currently in several cooperation projects covering a wide spectrum of research areas. Some of these projects, which are closely related to the proposed research, are summarized as follows.

Hardware/software codesign. ESLAB has been involved in a joint research project (COCODES), together with the Electronic System Design Lab at KTH, Synthesia AB, Ericsson Telecom, and Saab Dynamics, which is sponsored by NUTEK's Embedded Systems program. The project aims at the development of a design environment for embedded systems consisting of hardware and software components and are control and communication dominated. Based on an evaluation model, a specified system is partitioned into hardware and software domains and implementation details are added. We are also developing techniques to support re-partitioning and to handle changes in design requirements or of technology.

Application level programming of control systems. RTSLAB is involved in ISIS, a competence center for "information systems for integrated supervision and control", together with several other researcher groups at Linköping University and ABB Industrial Systems, ABB Robotics, Ericsson Utvecklings AB, Saab Au-

tomobile, Saab Dynamics, Saab AB, etc. The overall goal of ISIS is to provide competence that is useful for the design of complex industrial systems related to control and supervision. RTSLAB has also a past experience with multi-level architectures for process control.

Timing and functional analysis of embedded software systems. A Petri-net representation has been developed for capturing the sensing and control of a physical environment jointly by RTSLAB and ESLAB. The models are timed and the intention is to describe the controller and the controlled system using different model languages to achieve reusability, decomposition, and modularity. The models are automatically generated from process control software or system designs, and can be used for timing analysis of real time and process control system designs. In particular this is applied to systems described by process control languages. Process control languages are application specific high level languages, tailored for describing process control systems. At RTSLAB we have studied both standard process control languages and extensions, methods for error recovery and the integration of database technology in process control systems. Studies have also been made on how to achieve an engineering method, given end to end timing requirements on the system, which generates a reliable design of computational tasks in a fixed priority framework satisfying these requirements.

System engineering methods. RTSLAB participates in a larger European project which involves major aerospace industries. The project will develop a new standard for exchange of design data. RTSLAB's part is to develop the data model for design data. The scope of the project is the system development process - system requirement and functional analysis, and physical architecture design. The relevant tools for generating the design data are, e.g., Statemate, RDD-100, Core, MatrixX etc. Related to this is a project developing methods and tools for supporting the development and inspection process of software. By taking well known academic methods for verification and modifying them to be more suitable for engineering use, a method for supporting the inspection process has been developed. In relation to the focus of CESE this competence gives valuable insights into the industrial system development process, where the modelling and design tools mentioned earlier are to be used. The main industrial partners in the activities above are Saab Aerospace, Saab Dynamics and ABB Industrial Systems.

7. Industrial Cooperation

The main industrial partner of this project is Saab Dynamics AB. It has participated in the formulation of the research direction and identification of the main research issues of the project and will be involved partially in the execution of the research as well as its case studies and evaluations. The other industrial partners in the project, Saab AB and Volvo Technological Development, will be involved mainly in the problem formulation and evaluation part of the project. All industrial partners will be invited regularly to project meetings and will receive project reports and publications. The contact persons from the three companies will form a reference group of the project.

Contact information for the industrial partners is as follows:

Company	Contact Person(s)	E-mail	Telephone	Address
Saab Dynamics	Helge Persson Åke Johansson	helpe@weald .air.saab.se	013-186200	Saab Dynamics AB 581 88 Linköping
Saab AB	Dag Folkesson	dagfo@weald .air.saab.se	013-181855	Saab AB 581 88 Linköping
Volvo Technological Development	Jakob Axelsson	jaax@vtd .volvo.se	031-7724389	AB Volvo, Technological Development Chalmers Teknikpark 412 88 Göteborg

List of Appendices to the project “Hardware/Software Codesign of Real-Time Systems”

1. References.
2. Short resume of Prof. Zebo Peng.
3. Short resume of Dr. Anders Törne.
4. Supporting letter from Saab Dynamics.
5. Supporting letter from Volvo Technological Development.
6. Supporting letter from Saab AB will be sent in a separate envelop.

References

- [Axe95] J. Axelsson, "Analysis and Improvement of Task Schedulability in Hardware/Software Code-sign," Proc. 7th Euromicro Workshop on Real-Time Systems, pp. 276-283, Odense, June 14-16, 1995.
- [Axe96] J. Axelsson, "Hardware/Software Partitioning Aiming at Fulfilment of Real-Time Constraints," Journal of Systems Architecture 42(6-7):449-464, 1996.
- [Axe97a] J. Axelsson, "A Portable Model for Predicting the Size and Execution Time of Programs," Journal of Systems Architecture 43(1-5):211-213, 1997.
- [Axe97b] J. Axelsson, "Analysis and Synthesis of Heterogeneous Real-time Systems," Ph.D. Dissertation, Linköping University, Sweden, 1997.
- [Axe97c] J. Axelsson, "Architecture Synthesis and Partitioning of Real-Time Systems: A Comparison of Three Heuristic Search Strategies," Proc. 5th International Workshop on Hardware/Software Co-Design, pp. 161-165, Braunschweig, March 24-26, 1997.
- [Cam96] R. Camposano and J. Wilberg, "Embedded System Design," Journal on Design Automation for Embedded Systems, Vol. 1, pp.5-50, 1996
- [Ele96] P. Eles, Z. Peng, K. Kuchcinski and A. Doboli, "Hardware/Software Partitioning with Iterative Improvement Heuristics", Proc. 9th International Symposium on System Synthesis (ISSS'96), La Jolla, California, Nov. 6-8, 1996.
- [Ele97] P. Eles, Z. Peng, K. Kuchcinski and A. Doboli, "System Level Hardware/Software Partitioning Based on Simulated Annealing and Tabu Search," Journal on Design Automation for Embedded Systems, Vol. 2, pp.5-32, 1997.
- [Wol94] W. H. Wolf, "Hardware/Software Co-Design of Embedded Systems," Proceedings of the IEEE, 82(7):967-989, 1994.