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Distributed Real-Time Systems with Minimal Energy Consumption: Analysis and Synthesis

ARTES Project Proposal

Krzysztof Kuchcinski
Dept. of Computer Science
Lund Institute of Technology
Box 118, 221 00 Lund
E-mail: Krzysztof.Kuchcinski@cs.lth.se

Summary

This proposal describes the research project which concentrates on task scheduling for distributed heterogeneous computer architectures. The main emphasis of the proposed research is on such scheduling method which, in addition to fulfilling timing requirements of the final system, will minimize the energy consumption. This can be achieved by the scheduling method which selects tasks starting times as well as the processor voltage. Selecting the voltage of processors influences the task execution time and therefore consumed energy. This method will make it possible to execute selected tasks using slower processing modes while still satisfying all real-time constraints.

1. Problem statement

Much emphasis in real-time research is put on timing issues. Although timing is what characterizes a real-time system, increasingly important aspects are energy and power consumptions. Lower power consumption yields lower fabrication cost - cheaper package, cheaper power sources and higher reliability. Lower energy consumption yields lower operational costs for battery operated systems or longer life-span. These two issues are important in all types of applications, but especially for mobile computing & communication, deep-space exploration and medical implants.

The typical approach to power optimization in industry today is centered on “performance-power consumption trade-off”. High-performance systems are usually seen as energy and power eager, while low-power systems are perceived as being of low performance. Although performance is important, real-time applications mostly require predictability while minimizing other aspects influencing fabrication and operational cost. Resource cost, power/energy consumption together with reliability and maintainability are the factors which enforce the product cost.

In this context, there is a need for methods which target power and energy consumption minimization, while fulfilling certain timing constraints. Moreover, these methods are required throughout the whole design process. Approaches for power and energy reduction at lower abstraction levels have already been developed. At higher levels, such as system-level, there are rather few methods addressing these issues, and even fewer which take into account the specific features of real-time systems.

The goal of this project is to develop methods for designing real-time systems with low energy and low

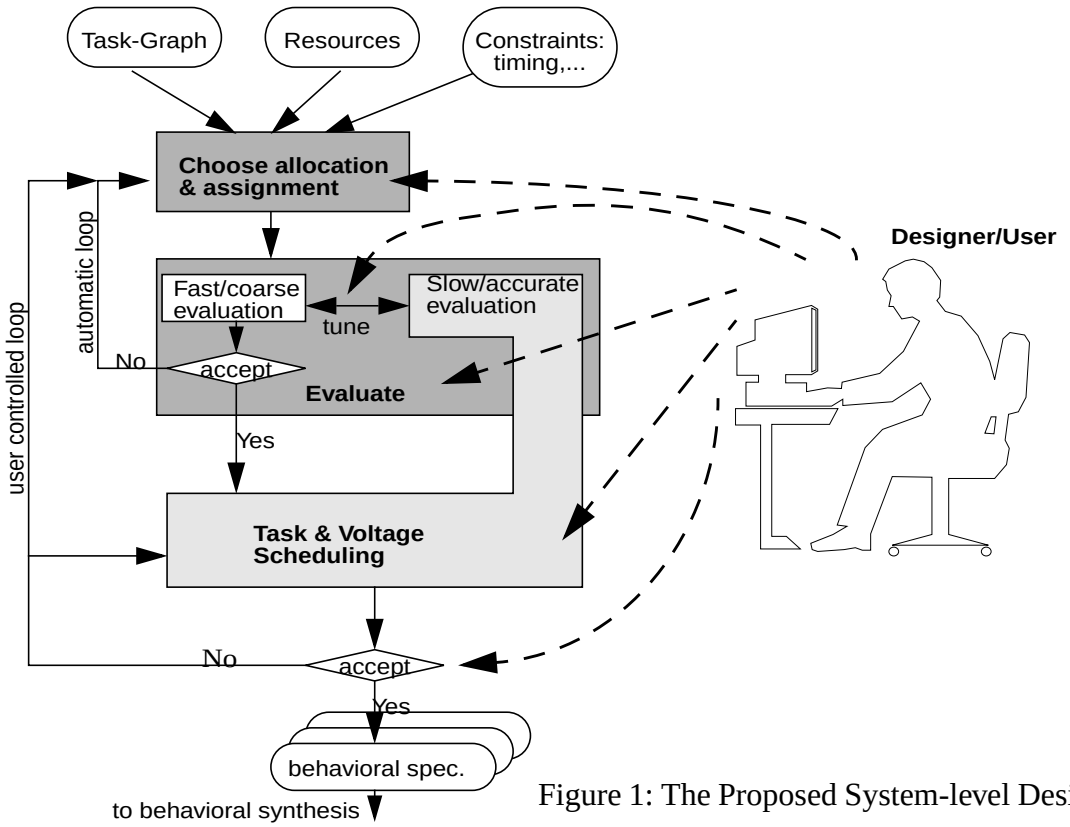

Figure 1: The Proposed System-level Design Flow

power consumption. The design methodology is focused from the start, at system level, on energy and power issues, while fulfilling the timing requirements.

2. Main ideas

We propose to investigate methods for designing real-time systems with low energy and low power consumption. We want to address these issues at system level, where we have the liberty to select the best architecture and schedule for our goal.

The design flow we propose will involve resource assignment and task-scheduling under timing constraints, while achieving minimal energy or/and peak power. In this context we make use of recent advances in the processor technologies, such as dynamic supply voltage processors and self-adjustable clock frequency processors. Assigning running voltages and frequencies is a problem referred to as “voltage scheduling” and makes the system design problem even harder. For this reason we propose an iterative design flow, involving user-controlled design space exploration (Figure 1).

Briefly, the design flow described in Figure 1 is a hybrid automatic - user centric flow. The resource allocation and task assignment can be specified partly by the designer or explored inside an automatic loop. In case of an automatic exploration a fast evaluator is needed, which can be specifically tuned for each particular design. The tuning is supervised by the user, which decides when the fast evaluator gives results which are good enough. Guiding the tuning is an accurate evaluator (which can be rather slow) involving actual scheduling of tasks and voltages on each processor. It is our belief that using the accurate evaluator inside the automatic loop will yield far to long execution times, thus the need of a less accurate but fast estimator. The final design step consists of task and voltage scheduling. Here, we decide the specific time moments and the voltages at which each processor has to run to fulfill the timing constraints (voltage scheduling).

Also, every task is assigned to their specific time intervals. Throughout the whole design flow, the designer has the possibility to control the process by various parameters or by forcing other solutions. The output of the proposed design flow consists of several behavioral level specifications which can be implemented as software or hardware. Not represented in the picture are the time/power/energy estimations for each task, obtained by estimators specific for each resource.

3. Expected results and impact

The expected contributions of this project are:

- A new approach to real-time system design, where, besides the timing aspects, other important issues are addressed throughout the design process. In particular, energy and power consumption are minimized while fulfilling the timing constraints. This approach will be implemented in a prototype system and tested on several real life and industrial examples.
- Better understanding of the possibilities for power and energy reduction for real-time systems implemented on variable voltage processors.
- Fast, system-level heuristic estimators for energy consumption, fine tunable for each particular design.

As for the efficiency of our method, some of our preliminary experiments on task and voltage scheduling only, show that for the tightest possible deadlines, up to 25% energy savings can be achieved. When the deadline are relaxed, even more energy can be saved. When combined with a well thought allocation and assignment, these savings can be even more dramatic.

4. Project plan

December 2000 - First prototype implementation of the tool for task scheduling as well as architecture and supply voltage selection.
Selection of realistic industry examples and preliminary evaluation of the tool.

December 2001 - The evaluation of the tool on the selected industrial examples and possible extensions based on the knowledge of the typical industrial problems.

June 2002 - Final evaluation of the tools and the methodology. Ph.D. presentation.

5. Preliminary budget

We apply for two years project with yearly support of 480 kkr which covers one graduate student, supervision and related traveling costs. Since Flavius Gruian did his Licentiate this year the two year period will be used to finish his Ph.D. dissertation.

Flavius Gruian, Tek. Lic.	80%	350 kkr
Krzysztof Kuchcinski, Prof.	10%	80 kkr
Travel costs		50 kkr
Total		480 kkr

6. Related research

Variable voltage processors are going today from the designers desk [1] to real products [2]. Methods addressing task and voltage scheduling for these types of processors have already appeared, but the majority deal with independent/non-communicating tasks [3][4]. Beside the mentioned approaches, few others address energy consumption as high as system-level design [6]-[10], but they often address very specific architectures. At lower abstraction levels, such as functional level, there are also a few techniques address-

ing multiple voltage hardware [11]. This problem, although similar in certain parts with ours, has some significant differences from voltage scheduling for variable voltage processors. In principle, building multiple supply voltage hardware implies fixing the voltage for each functional unit, voltage which will remain unchanged during the system lifetime. Using variable voltage processors makes the system more flexible, since it can be reprogrammed, but in the same time takes advantage of the low energy consumption at lower supply voltages.

7. Relation to the profile

The proposed project is related to ARTES profile is several ways. We consider implementation of the functionality specified as cooperating tasks with defined real-time constraints on a heterogeneous distributed architecture. This implementation has to fulfill, in the first place, all timing constraints, i.e., execution deadlines specified for a particular implementation. In addition to this usual requirement, we try to find out such implementation which reduces power and energy consumption. This goal extends traditional real-time system requirement and provide new methods and tools for systems which have demanding requirements on power consumption. Such systems becoming very common and include in first place battery driven systems but also a class of systems with limited power supply and cooling facilities.

8. Industrial relevance

Recently, processors which are able to adjust their supply voltage according to the required speed (clock frequency) have started to make their way from research to industry. They are more developed models of the processors supporting different “power-modes.” By running a processor at a lower voltage (and speed) one can save power and energy. The design technique presented in this document especially targets such variable voltage processors. Our belief is that more and more processors, starting from general purpose to microcontrollers, will be augmented with the hardware needed to take advantage of the variable supply voltage. Thus, our technique will be suited to a wide spectrum of applications requiring low energy and low power. Mobile computing and communication is probably the most relevant in this context. Other areas, although less common today, which can take advantage of the design method presented here are deep-space exploration and medical implants.

9. Relation to other SSF programs

This project area is connected to SSF program INTELECT (Integrated Electronic Systems) and particularly to the System-on-Chip research area. The selection of the distributed architecture, task assignment and finally scheduling of tasks and related communications is of great importance for system level design methodology. The combination of real-time and power/energy constraints is also typical for such systems which often need to be battery-driven and therefore require very careful design to meet both performance and timing constraints as well as power and energy consumption constraints.

10. Context

The proposed project will be carried out in the Embedded System Design group at the Dept. of Computer Science, Lund Institute of Technology. The research group consists currently of three graduate students and one professor. It is basically the CADLAB group from Linköping University which moved to Lund in January 2000. The department is a member of LUCAS center (Center for Applied Software Research) and the group benefits from these contacts.

The main research profile of the group is design of embedded computer systems. Such systems a characterized by heterogeneous constraints on timing, performance, power/energy consumption, memory, etc. The projects carried out in the group try to solve different aspects of the analysis and synthesis of such systems.

In addition to the proposed project we have a project on “System Partitioning and Scheduling with Memory Constraints” sponsored by SSF program INTELECT (Integrated Electronic Systems) and the project “Architectures for Conditions in Coarse Grain Programmable/ Reconfigurable Arrays”. Current proposed project was previously sponsored by WITAS, The Wallenberg laboratory for research on Information Technology and Autonomous Systems.

The group cooperates actively with WITAS laboratory at Linköping University in the project on developing embedded computer system for autonomous helicopter. There exist also good contacts with the ESD-Lab (Electronic System Design Laboratory) at KTH in terms of digital systems design. In terms of international cooperation we have good contacts with several European and US universities working in the area of design automation and embedded computer systems.

Industrial cooperation:

Bengt-Arne Molin
Axis Communications AB
Scheelevägen 16
S-223 70 Lund
Phone: +46 46 270 18 00
E-mail: bam@tde.lth.se

References

[1] K. Suzuki, S. Mita, T. Fujita, F. Yamane, F. Sano, A. Chiba, Y. Watanabe, K. Matsuda, T. Maeda, and T. Kuroda, “A 300MIPS/W RISC Core Processor with Variable Supply-Voltage Scheme in Variable Threshold-Voltage CMOS,” Proceedings of the IEEE Custom Integrated Circuits Conference 1997, pp. 587-590.

[2] “SH-1: SH7032/SH7034 Product Brief,” HITACHI Semiconductor Inc., 1997.

[3] I. Hong, Gang Qu, M. Potkonjak, and M.B. Srivastava, “Synthesis Techniques for Low-Power Hard Real-Time Systems on Variable Voltage Processors,” Proceedings of the 19th IEEE Real-Time Systems Symposium 1998, pp.178-187.

[4] I. Hong, D. Kirovski, Gang Qu, M. Potkonjak, and M. B. Srivastava, “Power Optimization of Variable Voltage Core-Based Systems,” Proceedings of the 35th Design Automation Conference 1998, pp. 176-181.

[5] F. Gruian and K. Kuchcinski, “Low-Energy Directed Architecture Selection and Task Scheduling for System-Level Design,” Proceedings of the 25th Euromicro Conference 1999, pp. 296-302.

[6] M. B. Srivastava, A. P. Chandrakasan and R. W. Brodersen, “Predictive System Shutdown and Other Architectural Techniques for Energy Efficient Programmable Computation,” IEEE Transactions on VLSI Systems, Vol.4 No.1, March 1996, pp. 42-51.

[7] C. Hwang and A. C. Wu, “A Predictive System Shutdown Method for Energy Saving of Event-Driven Computation,” Digest of Technical Papers of the IEEE/ACM International Conference on Computer-Aided Design 1997, pp. 28-32.

[8] T. Ishihara,H. Yasuura, “Voltage scheduling problem for dynamically variable voltage processors,” Proceedings of the 1998 International Symposium on Low Power Electronics and Design, 1998, pp 197-202.

[9] F. Yao, A. Demers, and S. Shenker, “A Scheduling Model for Reduced CPU Energy,” Proceedings of the 36th Symposium on Foundations of Computer Science, 1995, pp. 374-382.

[10] B. P. Dave, G. Lakshminarayana, and N. K. Jha, “COSYN: Hardware-Software Co-Synthesis of Embedded Systems”, Proceedings of the 34th DAC 1997, pp. 703-708.

[11] J.-M. Chang and M. Pedram, “Energy Minimization Using Multiple Supply Voltages,” IEEE Transactions on VLSI Systems, Vol. 5, No. 4, December 1997.

Appendices

Short CV of Krzysztof Kuchcinski

Krzysztof Kuchcinski received the M.Sc. and Ph.D. degrees in computer engineering and computer science from Gdansk University of Technology, Poland, in 1977 and 1984, respectively.He holds now a chair in Computer Science at Lund Institute of Technology (LTH), Lund, Sweden.

Until January 2000 he worked as an Associate Professor and later as the Professor of Computer Systems at the Department of Computer and Information Science, Linköping University, which he joint in 1986. During that time he was also a head of the CADLAB (Computer Aided Design Laboratory) group at this university. Prof. Kuchcinski co-authored a book on system design and published over 60 technical papers in international journals and conference. He was corecipient of two best papers awards at the EURO-DAC conference (European Design Automation Conference) in 1992 and 1994. He is currently the Editor-in-Chief of the Journal of Systems Architecture published by Elsevier Science and a member of several conference program committees as well as a reviewer for many international journals and conferences from the area of computer system design automation.

His main research interests include different aspects of embedded computer system analysis and synthesis as well as applications of constraint programming.

Supporting letters from industry

The letter from Bengt-Arne Molin (AXIS Communications AB) will be sent separately.