Artes Travel Report
European Test Workshop, Saltsjöbaden, Stockholm May 29 - June 1, 2001.

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I attended this workshop (it feels almost wrong to call a meeting with 130 people for a workshop) to learn more about techniques and problems of testing hardware components. The fist day I visit the tutorial "Test Challenges in Nanometer Technologies" by Sandip Kundu and Rajesh Galivanche at Intel Corporation. This workshop treated technology trends, defect mechanisms, circuit marginalities, current test trends and solution trends. The speakers were excellent and I really got to learn a lot of the things I hoped to learn from the workshop already during this tutorial. The second day the main workshop started with a keynote speech by R. Payne from Philips Semiconductors. He addressed the need for common platforms between different products to enhance testing. He also argued for the need of early silicon implementations to find specific faults early in the design process and stated that it is safer to remove hardware during design than to add new hardware. After that speech the main workshop started consisting of two parallel sessions, one containing papers from the academy and one containing industry reports. The fact that half of all presentations were made by people gave a nice mix of participants. This resulted in new ideas for the people from the academia during the industry presentations (this is the problem we want you to solve) and the right level of criticism during the presentations made by the academia. In many of the sessions it was allowed to ask questions during the presentation and 10 min was left in the end for both questions and discussions. That made it easier to put the presentation in a wider perspective in the area of testing and I think that most conferences would gain from such a schedule. To also make it possible for researchers to get feedback in an early phase of their projects a number of poster sessions were held during extended coffee breaks. Another event was the evening breakout session where 5 topics were presented by well known researchers and then everyone chose one topic and joined a brainstorm meeting around that topic. During the brainstorming wine was served and the results were summarized and presented at a specific common session the next day. The subjects of the normal sessions were: Testing of Analog and Digital Circuits (poster session), Defect-Oriented Testing, System-Level DFT (industrial practice), delay testing, Core-based Testing and P1500 (industrial practice), Scan Based Test & Testability (poster session), Case Studies, Full Scan (industrial practice), Analog and Mixed-Signal Testing, Transportation of Test Data (industrial practice), Test Generation and Testability Analysis (poster session), System-Level Testing, Hierarchical DFT (industrial practice), RTL Validation, DFT and TPG, Memory Testing (industrial practice), BIST and Power Consideration, BIST and Test Resource Partitioning, Mixed-Signal Testing (industrial practice), Logic BIST in Action (industrial practice). To summarize ETW, it is a nice workshop with a lot of well-known attendees from both the academia and industry, which gives a very nice atmosphere and interesting discussions. I learned a lot.