Travel Report from FPL 2005

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Introduction

International Conference on Field Programmable Logic and Applications (FPL) is the largest conference in the area of field-programmable logic. Developments in field-programmable logics have made them applicable for implementing large systems and accelerators. They are now employed in environments where hard real-time constraints must be guaranteed and for complex reconfigurable computing. The topics covered include reconfigurable architectures, applications, design methods and tools. Conference discussions usually include industrial applications, advanced electronic design automation (EDA) tools, research applications, novel systems architectures and educational experiences.

The Conference

The 15th edition of the International Conference on Field Programmable Logic and Applications tagged FPL 2005 took place in Tampere, Finland from August 24 to 26, 2005. It was organised by the Tampere University of Technology and co-sponsored by IEEE Circuits and Systems Society, IEEE Finland Section and Academy of Finland. There were two keynote addresses, "Computing Platform Requirements for Future Mobile Devices" by Yrjö Neuvo, Nokia, Finland and "Directions in FPGA Architectures and Design Methodologies" by Misha Burich, Altera, USA. There were ten presentation sessions, three poster sessions and one PhD forum. The most beneficial to me were sessions on Logic Synthesis, Video Processing Applications, Architectures and Systems, Multidimensional Processing and Compilation.

The Presented Paper

In this conference I presented a paper "Address Generation for FPGA Block RAM Accesses enabling Efficient Implementation of Real-Time Video Processing Systems". This paper described two approaches on accessing on-chip FPGA Block RAMs based on the global memory object architecture. A comparison of the experimental results obtained using the two approaches on real-time image processing systems design cases was included in the paper. There were two questions which were well answered and a comment.

Conclusions

I attended the conference with a colleague Niklas Lepistö and we had the opportunities of meeting many FPGA technology researchers. We discussed with both Altera and Xilinx representatives about FPGA memory architecture. Altera offers FPGAs with different memory sizes of a single chip while Xilinx offers only one memory size on-chip depending on the product family. The major reason for this difference is that Altera tends to provide a hardware platform that is more software friendly while Xilinx is dedicated to technology optimization by using single memory architecture per chip. This difference gives room for research opportunities: flexible memory architectures effectively optimised for process technology.

We had an excellent dinner after a nice Viking boat cruise.