

# **ARTES++ Travel Report to SELSE 3**

## **2007 IEEE Workshop on Silicon Errors in Logic – System Effects**

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### **1. Introduction**

The third Workshop on Silicon Errors in Logic – System Effects (SELSE 3) was held at the University of Texas at Austin. Modern electronic devices are becoming more susceptible to soft errors, caused by reduced dimensions, higher clock frequencies, and lower operating voltages. SELSE was started to provide a forum to discuss system effects of soft errors and techniques to deal with soft errors. SELSE had this year expanded the scope to also include other forms of silicon errors than soft errors, e.g., wearout faults.

### **2. Technical Program**

The technical program of SELSE 3 consisted of papers covering topics such as soft error characterization, wearout, error detection in processors, soft errors in memory, and system-level architecture. Two interesting panel discussions were held in addition to paper and poster presentations. I found one of the panel discussions, with the topic “*Silicon Errors in Modern Electronics: What are the Main Threats?*”, especially interesting. Panelists from academia and industry presented their view on which type of faults they expect to become the dominant cause of failures in future electronic circuits.

My contribution to the workshop was a paper titled “*Impact of Soft Errors in a Brake-by-Wire System*”, a joint work with Martin Sanfridson and my adviser, Professor Johan Karlsson. I received several questions and comments during the 30 minutes available for my presentation, feedback that will be of great value in our future work.

### **3. Conclusion**

SELSE 3 had a technical program consisting of interesting presentations from academia as well as industry. Besides providing me with feedback of my work, the workshop gave me a better knowledge of areas close to mine, e.g., circuit-level error detection. SELSE provided an excellent forum to discuss the effects of silicon errors and different techniques to deal with these errors.