Hierarchical Timed Automata for UPPAAL

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Abstract

In recent years, there have been a number of model-checking tools developed for timed automata. A common problem with these tools is that they can only accept a collection (or a product) of automata as input i.e. a flatten network of automata, which makes it difficult for the tools to model and debug industrial-sized systems.

Motivated by the notion of statecharts, we propose a hierarchical model for timed automata. The basic idea is the same as in statechart, namely, each state in a hierarchical automaton may be refined by another automaton. An operational semantics for hierarchical timed automata is presented, which is shown to be compositional. Based on the hierarchical model, a user-interface for the UPPAAL tool is being implemented, which allows the tool user to hide and abstract from internal structures of a system model in modelling and simulation, and more importantly to facilitate debugging, hierarchical traces may be provided as proofs to explain why a model satisfies certain properties.